

ACORN TECHNICAL MANUAL

**Versatile Interface Board .....200.009**

introduction .....page 2  
parts list .....page 3  
board layout .....page 4  
construction notes.....page 5  
circuit description .....page 6  
    INS8255 .....page 10  
    6522 .....page 11  
    MC6850 .....page 12  
applications programs ...page 14  
circuit diagram .....page 16

© Copyright Acorn Computers Ltd 1980.

Issue 1 Feb 1980

## INTRODUCTION

The Acorn Versatile Interface Board connects to the standard Acorn Computer Bus and provides interfaces via three integrated circuits listed below:-

### **6522**

This device provides two, eight bit parallel, TTL level, I/O ports, plus handshake lines, and a pair of interval timers for providing real time interrupts. One port connects to side B of the Acorn bus, the other going via a high current buffer to the front of the board where a 26 way connector is pin compatible with the Centronics or Anadex printers. The software to drive a printer via this interface already exists in the Cassette and Disk operating systems.

### **INS8255**

This device provides three eight bit ports of TTL level parallel I/O via a 34 way connector, two of these are programmable as input or output, the third is programmable in two groups of four as input or output.

### **MC6850**

This device provides serial interface in conjunction with an MC14411 baud rate generator under crystal control allowing transmission rates in the range 75 to 9600 baud to be selected. Edge connections on the front of the board provide an optically isolated 20 mA serial interface suitable for use with a standard teletype, and an RS232C connection. The RS232C interface requires a +-12V supply which may be connected via the front of the board or can be provided by an optional on board 5V to +-12V converter module. The serial data is also available at TTL levels and the control lines 'clear to send' and 'request to send' are available at RS232C or TTL.

As supplied the board is memory mapped into the lower half of page 0C. With the addition on board of a 74LS138 the board can be mapped into any half page in any of the lower eight blocks allowing many boards to be used as experimental interfaces or for the provision of extra printers etc.

Program examples of inputting and outputting serial data are supplied so that users may connect peripheral terminals such as teletypes.

**PARTS LIST FOR ACORN V.I.B**

PCB	Acorn computers Ltd. pt no 200.009	
IC1	74LS139 not supplied	
IC2	74LS138 decoder	and 16 pin socket
IC3	74LS139 decoder	and 16 pin socket
IC4	INS8255 P.I.A	and 40 pin socket
IC5	MC6850 ACIA	and 24 pin socket
IC6	MC1441 Baud rate generator	and 24 pin skt
IC7	6522 P.I.A	and 40 pin socket
IC8	74LS244 buffer	and 20 pin socket
IC9	74LS04 hex inverter	and 14 pin socket
IC10	TIL112 or TIL111 opto isolator	
Q 1,4	BCY70,BC309,etc P.N.P transistor,	2 off
Q 2,3,5-7	BC107,BC239,etc N.P.N transistor,	5 off
D 1,2,3	1N4148 diode	3 off
XTAL	1.8432 M Hz	
C1	15 uF,10V capacitor	
C2-8	47 nF capacitor	7 off
R1	15M resistor	not supplied
R2-4,8-11		
R15-21	4K7 resistor	13 off
R5,12	10K resistor	2 off
R6,13	1K resistor	2 off
R7,14	2K2 resistor	2 off
R15	270R resistor	1 off
R22	560R resistor	1 off

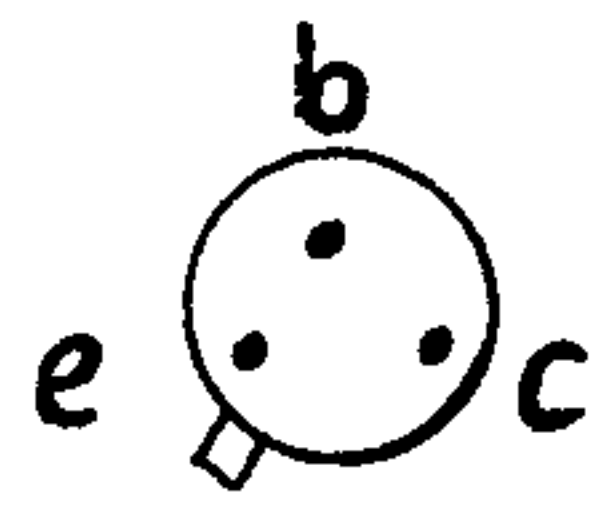
**OPTIONAL PARTS**

64 Way connector DIN 41612	, (for acorn bus), RS part 17-3704L
34 Way header plug	, (for 8255 ) , 3M part 3431-2302
34 Way mating ribbon cable skt,	(for 8255 ) , 3M part 3414-6000
26 Way right angle header plug,	(for printer ) , 3M part 3429-1302
26 Way mating ribbon cable skt,	(for printer ) , 3M part 3399-6000
+12v Converter	, (for RS232 use), ASTEC part AD1D 12A10

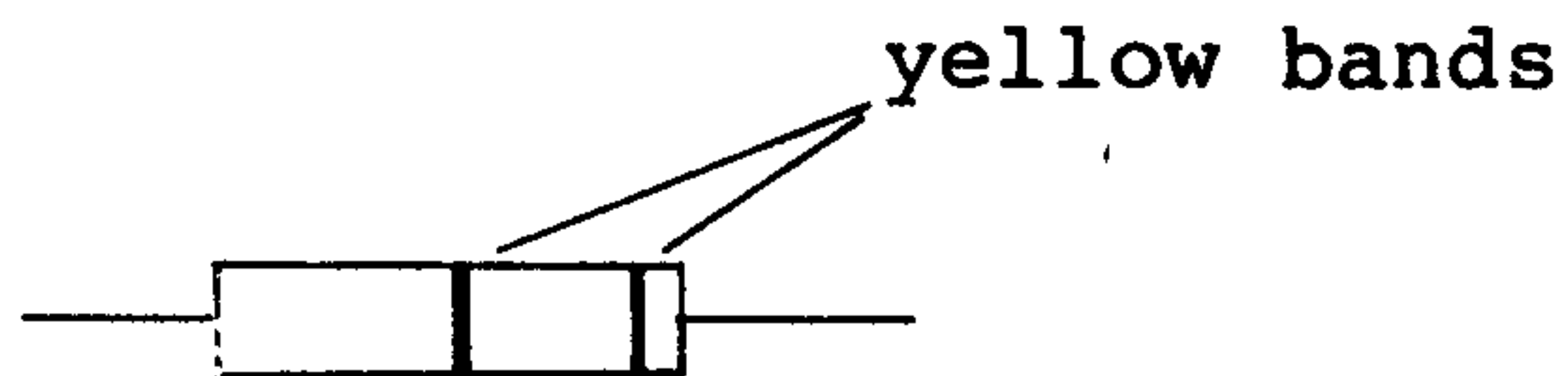
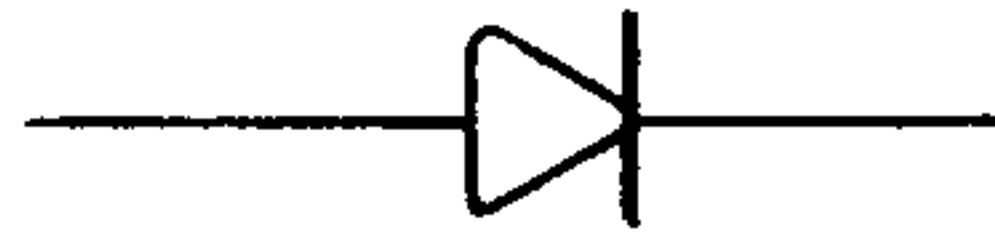


## CONSTRUCTION NOTES

Sockets are supplied for all IC's except IC10 and should be used .  
The system technical manual contains notes on soldering and component  
identification. The transistors and diodes supplied are shown below:-



transistors viewed from below  
, lead side.



IN4148 diode



## CIRCUIT DESCRIPTION

To use this board as supplied with the Acorn system a low for block zero signal must be present on pin 31A of the Acorn bus. This is provided by connecting pin 8 of IC9 to pin 31A of the connector on the 6502 C.P.U board. The 5 volt regulator and the electrolytic capacitor must be removed from the C.P.U board. Power is then supplied to all boards via their connectors +5V to pin 1A , 0V to pin 32A on all boards. A fully populated V.I.B will require a supply of 0.5 amps at 5V.

As supplied the V.I.B is memory mapped into page 0C (ie. in block zero) by using the links associated with IC's 2 and 3 this may be changed (see figure 1). When changing the location of the board in memory reference should be made to the memory map of the system (see system manual ) to ensure that no conflict occurs. The position of the board should not be changed if the printer is to be driven by the COS or DOS software. With the addition of a second 74LS138 in the position marked IC1 on the board the V.I.B may be mapped to occur in any of the lower eight blocks of memory (see figure 1). The three interface chips then occur in the selected half page as shown:-

		as supplied	modified
IC7	6522	0C00	base +00
IC5	MC6850	0C20	base +20
IC4	INS8255	0C40	base +40

These are the base addresses for the IC's and their registers will occur in the area of memory above these bases, the relevant sections should be consulted for details of these registers.

The interrupt lines from the 6522 and the MC6850 are available in the lower right hand corner of the board and may be linked to the required interrupt lines on the Acorn bus as shown in figure 2. These interrupt wires should be linked across on side B of the connectors on the Acorn backplane to boards that require them.

FIGURE 1a BLOCK SELECT OPTIONAL

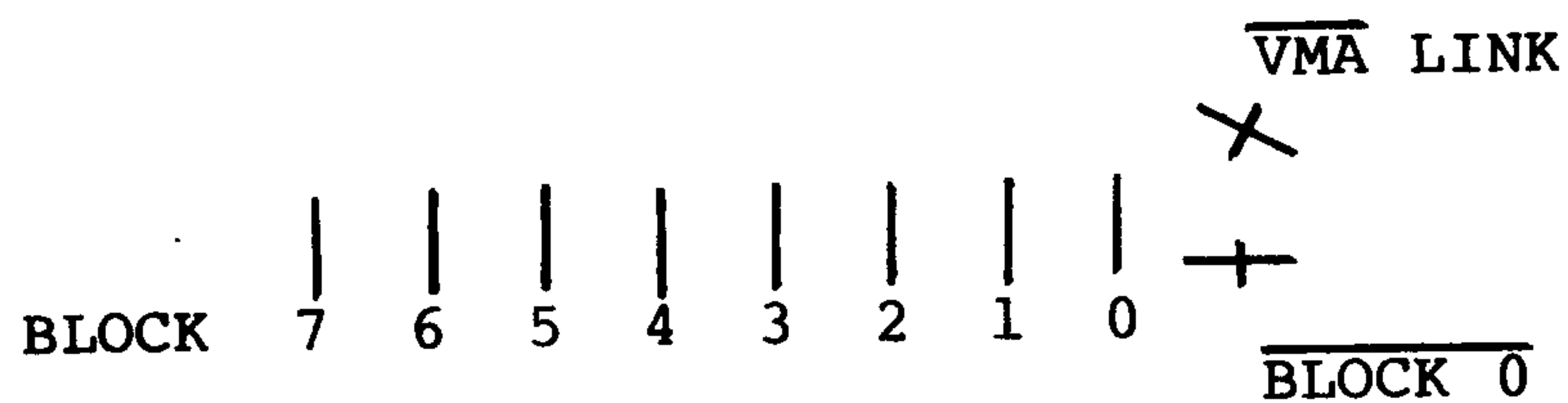


FIGURE 1b PAIR OF PAGES SELECT

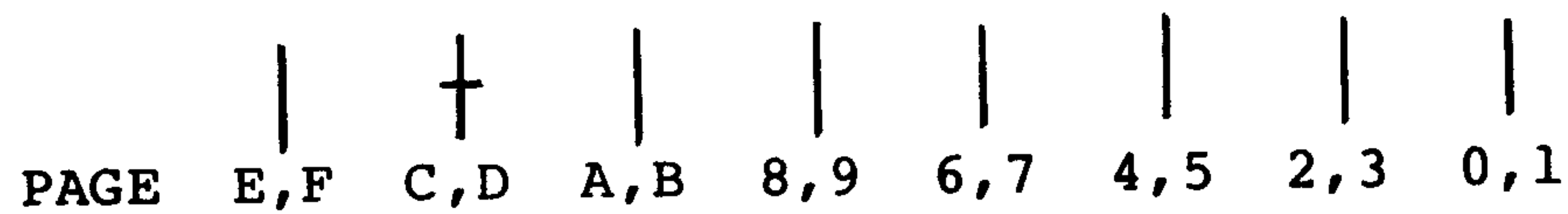


FIGURE 1c HALF PAGE SELECT

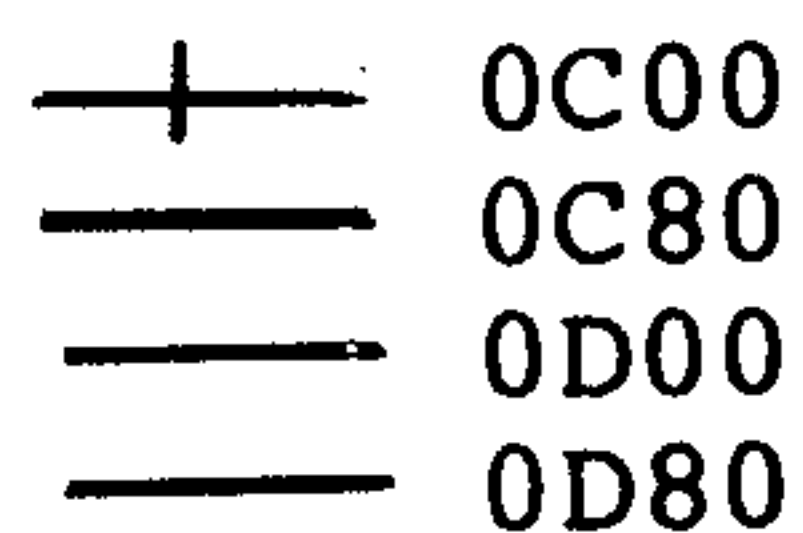
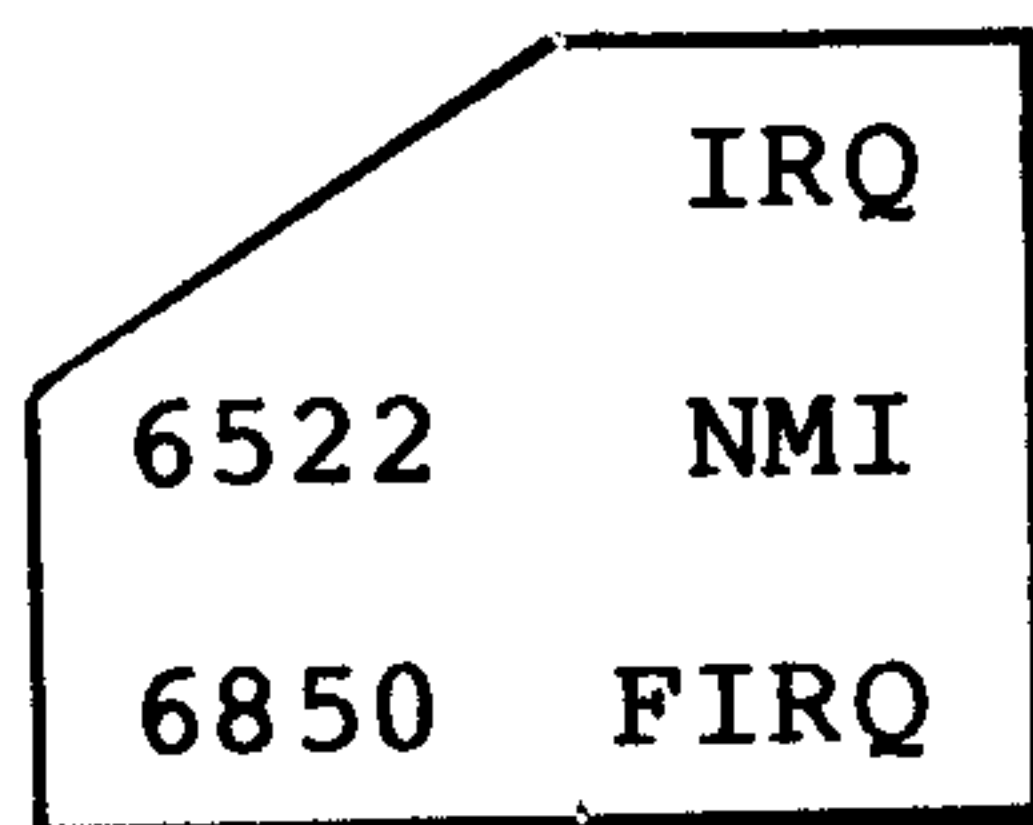
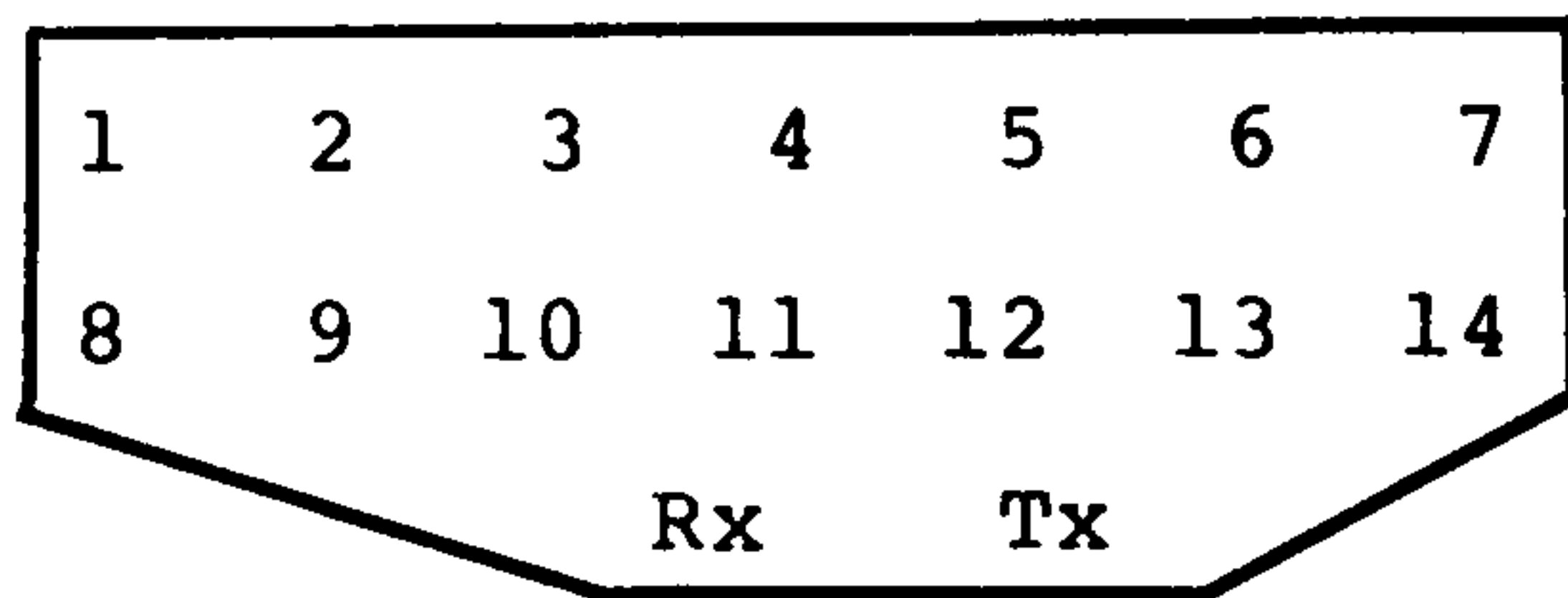


FIGURE 2 INTERRUPT SELECT



N.B (FIRQ used on 6809 system)

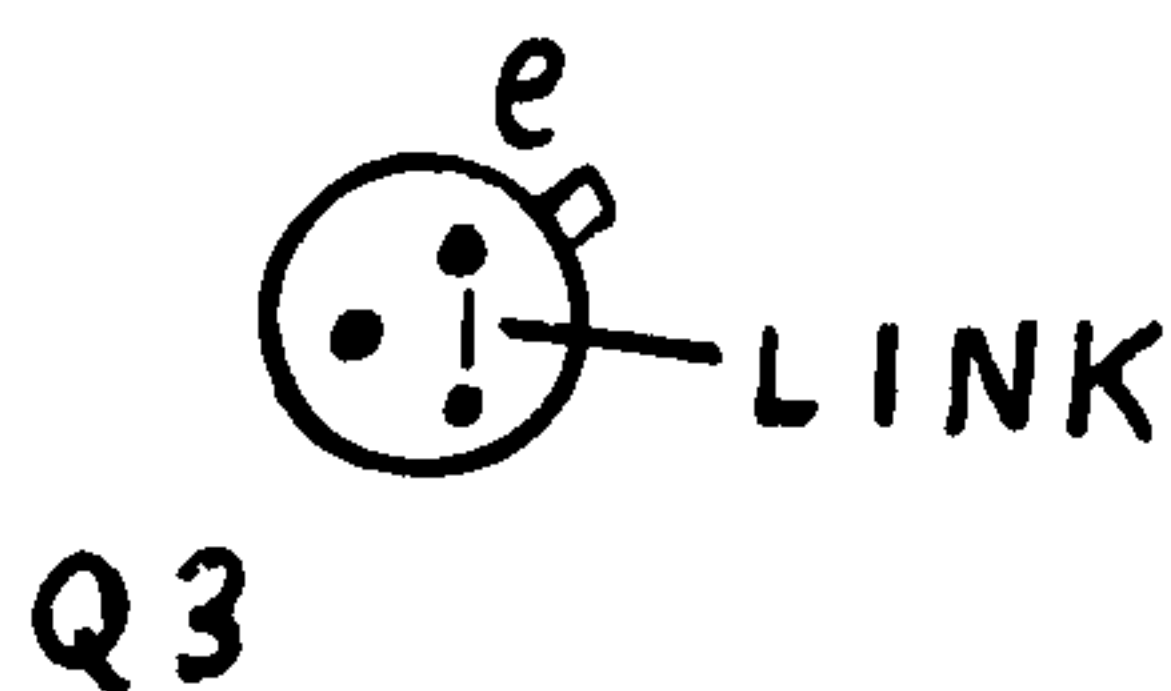
The last set of option links on the board select the baud rate to the MC6850 supplied by the MC14411 baud rate generator. The 6850 has two clock inputs one to define the transmission rate, and the other for the reception rate. The 6850 then divides this rate by 16 or 64 to derive the baud rate of the data. As supplied the board is linked for 110 baud operation with the MC6850 programmed for a divide by 64 clock. This may be changed by altering the links on the board as shown:-



LINK	CLOCK Baud	/16 Baud	/64 Baud
1	307.2k	19.2k	4.8k
2	153.6k	9.6k	2.4k
3	38.4k	2.4k	600
4	19.2k	1.2k	300
5	4.8k	300	75
6	8.6k	538	134
7	230.4k	14.4k	3.6k
8	614.4k	38.4k	9.6k
9	76.8k	4.8k	1.2k
10	12.8k	800	200
11	9.6k	600	150
12	7.0k	440	110
13	115.2k	7.2k	1.8k
14	460.8k	28.8k	7.2k

20mA loop operation

Referring to the component layout pins 2 and 4 of the serial interface provide an optically isolated 20mA passive input. In this mode the transmitting device must provide the current; with the addition of R22 the board provides an active input. The transmitting device should then be connected between pins 2 and 3. Pins 6 and 8 on the serial interface are an active 20mA output. For operation in the 20mA loop mode the CTS input to the MC6850 must be disabled, if the components have been fitted in the RS232C circuit this may be done by linking pins 9 and 5 on the serial interface. If these components have not been fitted the collector and emitter connecting pads for Q3 should be linked with a piece of wire as shown here.





### RS232C operation

For RS232C operation the link that lies between the leads of the crystal should be cut on the underside of the board and the link beside IC9 should be made. Power for the RS232C circuit may be provided by an on board +5V to +-12V converter (AD1D12A10) or supplied via the front of the board (+12V to pin 5, -12V to pin 1, 0V to pin 7)

Connections for RS232C operation are then available as follows:-

Pin 14	data output
Pin 12	data input
Pin 9	clear to send input
Pin 11	request to send output
Pin 7,10,13	common 0v

### PRINTER INTERFACE

The printer is controlled via port A of the 6522 the data and strobe lines are buffered by the 74LS244. The connections available on the front of the board may be taken by insulation displacement connectors and ribbon cable to a Centronics printer. The following connections are available on the front of the board for connection to a printer;

Pin 2-24	Even numbers 0v
Pin 1	Negative strobe
Pin 3-15	Odd numbers, Data 0-6
Pin 19	Negative acknowledge
Pin 21	Busy

The cassette and disk operating systems contain software to drive a printer via this interface. The system manual should be consulted for details of how to control the printer.

## INS8255

Connections to the INS8255 are available via a 32 way connector pad adjacent to the IC on the board. The electrical specification of the INS8255 connections are as follows.

Input low voltage	0.8 V max
Input high voltage	2.0 V min
Output low voltage	0.4 V max Iol=1.6 mA
Output high voltage	2.4 V min Ioh= -50 uA
Darlington drive current	2 mA Voh=1.5 V Rext=390R

When fitted the INS8255 will typically draw 40 mA from the supply rails.

The INS8255 has three basic modes of operation that can be selected by the system software. In the first mode ( mode 0), the INS8255 provides simple input and output operations for three 8-bit ports. Data is simply written to or read from a specified port without the use of 'handshaking' signals. In the second mode ( mode 1), the INS8255 enables the transfer of input/output data to or from a specified 8-bit port (A or B) in conjunction with strobes or 'handshaking' signals available from port C. In the third mode ( mode 2), the INS8255 enables communications with a peripheral device or structure via one bidirectional 8-bit bus port ( port A). 'Handshaking' signals are provided over lines of port C in this mode to maintain proper bus flow discipline.

The first of these modes is described in more detail here. The data sheet for the INS8255 should be consulted for details of the other modes. The registers of the INS8255 occur in the following places in memory:

Port A	0C40	base +40
Port B	0C41	base +41
port C	0C42	base +42
Control register	0C43	base +43

It should be noted that whenever the control register is loaded with a new mode definition all output registers are reset. The data written to the Control word register may have one of two uses: if the top bit is set the data is a new mode definition for the INS8255, if the top bit is clear the data is an instruction to set or clear a bit in port C. The control word register is write only the bits in it have the following significance.

Bit 7	mode set flag =1
Bit 6	mode control=0 for mode 0
Bit 5	mode control=0 for mode 0
Bit 4	port A control 1=input, 0=output
Bit 3	port C (upper) 1=input, 0=output
Bit 2	mode control=0 for mode 0
Bit 1	port B control 1=input, 0=output
Bit 0	port C (lower) 1=input, 0=output

If the top bit is clear the following meanings are assigned.

Bit 7	bit set/reset flag=0
Bit 6-4	not used
Bit 3-1	bit select (000=bit0, 001=bit1, etc)
Bit 0	0=bit reset, 1=bit set

On reset all the internal registers of the INS8255 are logical 0. This sets ports A,B and C to the high impedance input mode.

Once the mode has been defined the ports may be written to or read from at the appropriate locations in memory, and the control word register may be used in its bit set/reset mode to set or reset individual bits in port C.

### 6522

Connections to the 6522 are available at the front of the board from port A in a configuration suitable for use as a printer interface, and on side B of the edge connector to the Acorn bus for port B. The electrical specification for these connections are:

Side B of 64 way edge connector.

Input high voltage	2.4 V min
Input low voltage	0.8 V max
Output low voltage	0.4 V max Iol=1.6 mA
Output high voltage	2.4 V min Ioh=-100 uA

Printer output from front of board.

Buffered output low volts	0.5 V max Iol=24 mA
Buffered output high volts	2.4 V min Ioh=-15 mA

When fitted the 6522 will typically draw 25 mA from the supply.

The 6522 interfaces primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either input or output. Two control lines per port can be used to control handshaking of data via the port, and to provide interrupts. Peripheral I/O lines can be selectively controlled by interval timers to generate programmable frequency square waves and/or to count externally generated pulses. A shift register allows serialisation of data under control of the counters.

The use of the 6522 for parallel I/O is described in more detail here. The data sheet for the 6522 should be consulted for details of the other modes. The registers of the 6522 occur in the following places in memory:



Data register A	0C00	base +00
Data register A	0C01	base +01
Data direction B	0C02	base +02
Data direction A	0C03	base +03
Timer 1 low counter	0C04	base +04
Timer 1 high counter	0C05	base +05
Timer 1 low latch	0C06	base +06
timer 1 high latch	0C07	base +07
Timer 2 low counter	0C08	base +08
Timer 2 high counter	0C09	base +09
Shift register	0C0A	base +0A
Auxiliary control	0C0B	base +0B
Peripheral control	0C0C	base +0C
Interupt flags	0C0D	base +0D
Interupt enable	0C0E	base +0E
Data A (no handshake)	0C0F	base +0F

On reset all internal registers of the 6522 are logical 0 (except T1, T2 and SR). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupts from the chip. To use the ports in a simple I/O mode with no handshake the data direction register associated with each I/O register must be programmed. A byte is written to each of the data direction registers to specify which lines are to be inputs and which outputs. Placing a '0' in a bit in the Data Direction Register causes the corresponding line to act as an input, while a '1' causes it to act as an output. Writing to either of the port registers will now cause the lines that are programmed as outputs to follow the state of the corresponding bits in the port, lines programmed as inputs will not be affected. Reading from either of the ports returns a byte reflecting the status of the corresponding lines which are programmed as inputs. Lines programmed as outputs will return status of the output pin for port A, and the status of the output data register for port B.

### MC6850

Conetions to the MC6850 are available via the front of the board and are buffered for 20 mA loop or RS232C operation. The following conections are available on the front of the board;

PIN 1	-12v
Pin 2	TTY -ve input ,opto isolated
Pin 3	0v
Pin 4	TTY +ve input ,opto isolated
Pin 5	-12v Supply
Pin 6	TTY -ve output
Pin 7	0v
Pin 8	TTY +ve output
Pin 9	NCTS RS232c input
Pin 10	0v
Pin 11	NRTS RS232c output
Pin 12	RS232c Data input
Pin 13	0v
Pin 14	RS232c Data output
Pin 15-22	Not conected

The 6850 provides serial I/O with independent send and receive data rates. A programmable control register provides, variable word lengths, clock division ratios, transmit control, receive control, and interrupts. A status register provides an interrupt flag and frame, parity and overrun error flags.

The registers of the 6850 occur in the following places in the memory map;

Transmit data register	0C21	base +21	write only
Receive data register	0C21	base +21	read only
Control register	0C20	base +20	write only
Status register	0C20	base +20	read only

After a hardware reset and before the 6850 may be used a master reset must be sent to the 6850 by writing 03 into its control register. The control register should then be programmed to configure the required options, the bits in the control register have the following significance;

Bit 0,1	Counter divide control
Bit 2-4	Word control
Bit 5,6	Transmit control
Bit 7	Receiver interrupt enable

These bits select the options as follows;

#### COUNTER DIVIDE CONTROL

CR1	CR0	Function
0	0	Divide by 1 (externally synchronised clock)
0	1	Divide by 16
1	0	Divide by 64
1	1	Master reset

The selection of baud rates is described in the circuit description.

#### WORD CONTROL

CR4	CR3	CR2	Function
0	0	0	7 bits, even parity, 2 stop bits
0	0	1	7 bits, odd parity, 2 stop bits
0	0	0	7 bits, even parity, 1 stop bit
0	1	1	7 bits, odd parity, 1 stop bit
1	0	0	8 bits, 2 stop bits
1	0	1	8 bits, 1 stop bit
1	1	0	8 bits, even parity, 1 stop bit
1	1	1	8 bits, odd parity, 1 stop bit

#### TRANSMIT CONTROL

CR6	CR5	Function
0	0	NRST low, transmit interrupt disabled
0	1	NRST low, transmit interrupt enabled
1	0	NRST high, transmit interrupt disabled
1	1	NRST low, transmit break level on data line, transmit interrupt disabled.



## RECEIVE INTERRUPT ENABLE

CR7	Function
0	Interrupt disabled
1	Interrupt enabled

The status register contains the following flags;

Bit 0	Receive data register full
Bit 1	Transmit data register empty
Bit 2	Not data carrier detect
Bit 3	Not clear to send
Bit 4	Framing error
Bit 5	Receiver overrun
Bit 6	Parity error
Bit 7	Interrupt request

The program listed here demonstrates the use of the 6850 in communication with a teletype.

\*

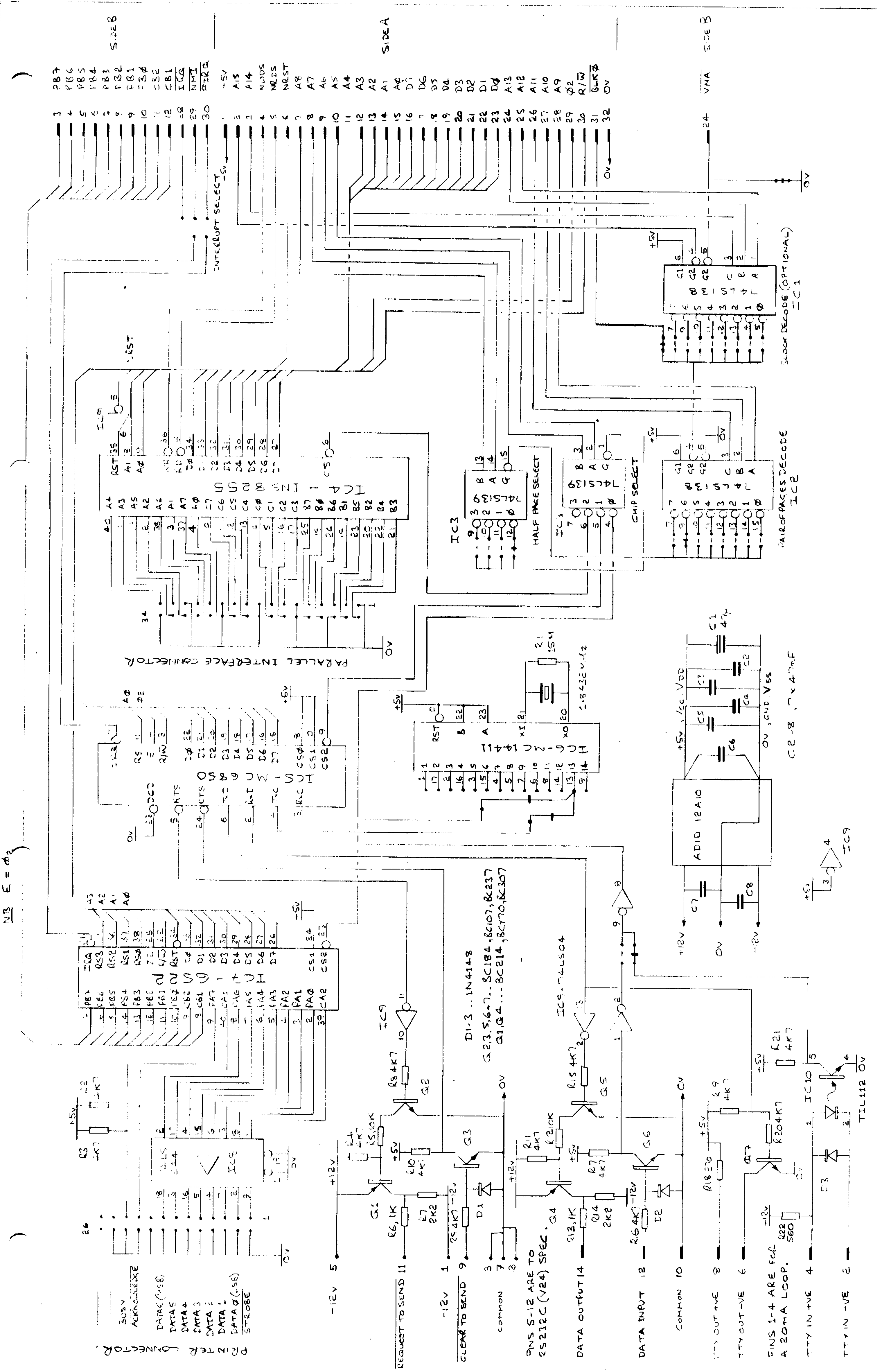
TTY

```
0010: 0200          TTY  ORG  $0200
0020:                *****
0030:                *
0040:                * TELETYPE INTERFACE *
0050:                *
0060:                * example program *
0070:                *
0080:                *****
0090: 0200          PORT  *   $0C21  6850 Data register
0100: 0200          STATUS *   $0C20  6850 Status register
0110: 0200 A9 03    SETUP LDAIM $03  Master reset of 6850
0120: 0202 8D 20 0C STA  STATUS
0130: 0205 A9 02    LDAIM $02  Receive interrupt disable
0140:                NRTS low, Transmit interrupt disable
0150:                Seven bits, Even parity, Two stop bits
0160:                Counter divide by 64
0170: 0207 8D 20 0C STA  STATUS
0180: 020A 60        RTS
0190: 020B A9 01    READ  LDAIM $01
0200: 020D 2C 20 0C WAITIN BIT  STATUS
0210: 0210 F0 FB    BEQ   WAITIN Wait for Receive Data Register Null
0220: 0212 AD 21 0C LDA  PORT  Load byte and return
0230: 0215 60        RTS
0240: 0216 48        SEND  PHA
0250: 0217 A9 02    LDAIM $02
0260: 0219 2C 20 0C NOTCLR BIT  STATUS
0270: 021C F0 FB    BEQ   NOTCLR Wait for Transmit Data Register Empty
0280: 021E 68        PLA
0290: 021F 8D 21 0C STA  PORT  Store byte and return
0300: 0222 60        RTS
ID
```

```

0010: 0200          PEXAMP ORG    $0200
0011:                *****
0012:                * PRINTER DRIVER *
0013:                * example program *
0014:                *****
0020: 0200          VIA      *    $0C00
0030: 0200          PCR      *    VIA    +0C Peripheral control register
0040: 0200          DDRA     *    VIA    +03 Data direction register
0050: 0200          ORA      *    VIA    +01 Output register
0060: 0200 48          PRINT  PHA
0070: 0201 C9 02          CMPIM $02
0080: 0203 F0 23          BEQ   PRINB  Switch printer on
0090: 0205 C9 03          CMPIM $03
0100: 0207 F0 30          BEQ   PRINC  Switch printer off
0110: 0209 AD 0C 0C  PRINA  LDA   PCR    is printer on ?
0120: 020C 29 0E          ANDIM $0E
0130: 020E F0 27          BEQ   PRINL  Printer is off so exit
0140: 0210 68          PLA
0150: 0211 2C 01 0C  PRINP  BIT   ORA    Wait for ready
0160: 0214 30 FB          BMI   PRINP
0170: 0216 8D 01 0C          STA   ORA    Output byte
0180: 0219 48          PHA
0190: 021A AD 0C 0C          LDA   PCR
0200: 021D 29 F0          ANDIM $F0
0210: 021F 09 0C          ORAIM $0C
0220: 0221 8D 0C 0C          STA   PCR    Pulse strobe low
0230: 0224 09 02          ORAIM $02    Strobe high again
0240: 0226 D0 0C          BNE   PRING  Branch always
0250: 0228 A9 7F          PRINB  LDAIM $7F  This switches the printer output on
0260: 022A 8D 03 0C          STA   DDRA
0270: 022D AD 0C 0C          LDA   PCR
0280: 0230 29 F0          ANDIM $F0
0290: 0232 09 0E          ORAIM $0E
0300: 0234 8D 0C 0C  PRING  STA   PCR
0310: 0237 68          PRINL  PLA
0320: 0238 60          RTS
0330: 0239 AD 0C 0C  PRINC  LDA   PCR    This switches the printer output on
0340: 023C 29 F0          ANDIM $F0
0350: 023E B0 F4          BCS   PRING
ID

```



N.B. E = 0

ISSUE	A	B	1	2	DATE	03-10-79	26-10-79	04-01-80	3-3-80
DATE	03-10-79	26-10-79	04-01-80	3-3-80					
© COPYRIGHT 1979 ACORN COMPUTERS LTD 4 A, MARK CAMBRIDGE TEL 0223-314772									
DESIGN CBT					TITLE VERSATILE INTERFACE BOARD				
REF 200.009/C					ACORN COMPUTERS LTD				